

**CLAIMS****What is claimed is:**

- 1 1. A multi-phase sampling system having an odd number of evenly distributed  
2 clock phases, the clock phases being generated by a multi-phase clock generator, the  
3 system comprising:  
4 a plurality of samplers, each of the samplers sampling a same input data signal  
5 when a clock signal of one of the respective phases is received by the respective  
6 sampler, each sampler sampling a transition and data of the input data signal, each  
7 sampler outputting a respective output signal.
- 1 2. The multi-phase system of claim 1, wherein the multi-phase system comprises  
2 an odd number of said samplers.
- 1 3. The multi-phase system of claim 1, further comprising:  
2 phase error determination circuitry, the phase error determination circuitry  
3 receiving the respective output signals and making a respective phase error  
4 determination based on each of the respective output signals.
- 1 4. The multi-phase system of claim 3, further comprising:  
2 phase shifting circuitry, the phase shifting circuitry shifting one or more of the  
3 phases in accordance with the respective phase error determinations.
- 1 5. The multi-phase system of claim 1, wherein the multi-phase system is a  
2 receiver in communication with a multi-phase transmitter.
- 1 6. The multi-phase system of claim 1, wherein the multi-phase system is a  
2 transmitter.

1 7. The multi-phase system of claim 5, wherein the multi-phase system further  
2 comprises:  
3 phase error determination circuitry, the phase error determination circuitry  
4 receiving the respective output signals and making a respective phase error  
5 determination based on each of the respective output signals, and wherein some of the  
6 phase error determinations correspond to phase errors of the multi-phase receiver and  
7 wherein some of the phase error determinations correspond to phase errors of the  
8 multi-phase transmitter.

1 8. The multi-phase system of claim 7, further comprising:  
2 phase shifting circuitry, the phase shifting circuitry shifting one or more of the  
3 phases of the multi-phase receiver in accordance with the respective phase error  
4 determinations.

1 9. The multi-phase system of claim 7, wherein the phase error determinations  
2 that correspond to phase errors of the multi-phase transmitter are fed back to the  
3 multi-phase transmitter to enable phase shifting circuitry of the multi-phase  
4 transmitter to shift one or more of the phases of the multi-phase transmitter in  
5 accordance with the respective phase error determinations of the multi-phase  
6 transmitter.

1 10. A multi-phase system comprising a multi-phase clock signal generator that  
2 generates at least a first clock signal having a first phase, a second clock signal having  
3 a second phase, and a third clock signal having a third phase, the first, second and  
4 third phases being different from each other, the apparatus comprising:  
5 a first sampling device that receives a first data signal and the first clock  
6 signal, the first sampling device comprising first sampling logic configured to sample  
7 the first data signal when the first clock signal is received by the first sampling device  
8 and to cause a first output signal to be output from the first sampling device;  
9 a second sampling device that receives the first data signal and the second  
10 clock signal, the second sampling device comprising second sampling logic  
11 configured to sample the first data signal when the second clock signal is received by  
12 the second sampling device and to cause a second output signal to be output from the  
13 second sampling device;

14 a third sampling device that receives the first data signal and the third clock  
 15 signal, the third sampling device comprising third sampling logic configured to  
 16 sample the first data signal when the third clock signal is received by the third  
 17 sampling device and to cause a third output signal to be output from the third  
 18 sampling device;  
 19 phase error determination circuitry configured to determine a first phase error  
 20 indication associated with the first output signal, a second phase error indication  
 21 associated with the second output signal and a third phase error indication associated  
 22 with the third output signal; and  
 23 phase shifting circuitry configured to shift at least one of the first, second or  
 24 third phases in accordance with the respective first, second, or third phase error  
 25 indications.

1 11. The apparatus of claim 10, wherein at least the first phase error indication is  
 2 used by the phase shifting circuitry to phase-lock the multi-phase clock signal  
 3 generator, and wherein the phase shifting logic shifts the second and third phases in  
 4 accordance with the second and third phase error indications, respectively.

1 12. The apparatus of claim 10, wherein the first, second and third phase error  
 2 indications are used by the phase shifting circuitry to phase-lock the multi-phase clock  
 3 signal generator, and wherein the phase shifting circuitry shifts the first, second and  
 4 third phases in accordance with the first, second and third phase error indications,  
 5 respectively.

1 13. The apparatus of claim 10, wherein the phase shifting circuitry includes first,  
 2 second and third charge pumps that perform modulo binning of the first, second and  
 3 third phase error indications, respectively, to obtain first, second and third phase  
 4 shifting values, and wherein the phase shifting circuitry shifts the first, second and  
 5 third phases in accordance with the obtained first, second and third phase shift values,  
 6 respectively.

1 14. The apparatus of claim 10, wherein the phase error determination circuitry  
 2 comprises logic that is configured based on an Alexander Phase Determination Truth  
 3 Table algorithm.

1 15. The apparatus of claim 13, wherein the phase shifting logic further includes at  
2 least first and second phase shifters configured to operate on the first and second  
3 clock signals, respectively, the first and second phase shifters receiving outputs from  
4 the first and second charge pumps, respectively, the first and second phase shifters  
5 shifting the first and second phases, respectively, in accordance with the outputs  
6 received from the first and second charge pumps, respectively.

1 16. The apparatus of claim 15, wherein the apparatus is incorporated into a  
2 receiver, and wherein the phase shift adjustments cause the first and second clock  
3 signals to arrive at the first and second sampling devices, respectively, at particular  
4 points in time to thereby cause the first and second sampling devices to sample the  
5 first data signal at correct points in time, the first data signal corresponding to a signal  
6 transmitted by a transmitter.

1 17. The apparatus of claim 15, wherein the apparatus is comprised by a receiver,  
2 and wherein the phase shift adjustments cause the first and second clock signals to  
3 arrive at the first and second sampling devices, respectively, at particular points in  
4 time to cause the first and second sampling logic to optimally sample the first data  
5 signal, the first data signal corresponding to a signal transmitted by a transmitter, the  
6 transmitter being a multi-phase system comprising a multi-phase clock generator that  
7 generates at least third, fourth, fifth, sixth and seventh clock signals having third,  
8 fourth, fifth, sixth and seventh phases, respectively, the third, fourth, fifth, sixth and  
9 seventh phases being different from each other, and wherein the phase error  
10 determination logic is also configured to determine one or more phase error  
11 indications associated with events occurring in the transmitter, and wherein the phase  
12 error indications determined to be associated with events occurring in the transmitter  
13 are transmitted by the receiver to the transmitter to enable the transmitter to adjust the  
14 third, fourth, fifth, sixth and seventh phases to eliminate phase errors in the third,  
15 fourth, fifth, sixth and seventh clock signals.

18. The apparatus of claim 15, wherein the apparatus is comprised by a transceiver, the transceiver comprising a local receiver and a local transmitter, and wherein the phase shift adjustments cause the first and second clock signals to arrive at the first and second sampling devices, respectively, at particular points to cause the first and second sampling logic to optimally sample the first data signal, and wherein the first data signal corresponds to a signal transmitted by a remote transmitter, the remote transmitter being a multi-phase system comprising a multi-phase clock generator that generates at least third, fourth, fifth, sixth and seventh clock signals having third, fourth, fifth, sixth and seventh phases, respectively, the third, fourth, fifth, sixth and seventh phases being different from each other, and wherein the phase error determination logic is also configured to determine one or more phase error indications associated with events occurring in the remote transmitter, and wherein the phase error indications determined to be associated with events occurring in the remote transmitter are transmitted by the receiver to the remote transmitter to enable the remote transmitter to adjust the third, fourth, fifth, sixth and seventh phases to eliminate phase errors in the third, fourth, fifth, sixth and seventh clock signals, respectively.

19. An apparatus for sampling signals in a first multi-phase system, the first multi-phase system comprising a multi-phase clock signal generator that generates  $m$  clock phases, each clock phase being different, the apparatus comprising:

$n$  sampling devices,  $m$  and  $n$  being integers that are relatively prime, wherein  $n$  corresponds to a number of clock phases of a second multi-phase system and is equal to or greater than 3, each of the sampling devices sampling a first data signal when one of the  $m$  clock signals is received by the sampling device and outputting an output signal;

phase error determination circuitry, the phase error determination circuitry being configured to determine a phase error indication associated with each output of the  $n$  sampling devices;

$m + n$  modulo binning devices, and wherein  $m$  of the modulo binning devices perform binning of the phase error indications associated with the outputs of the  $m$  sampling devices to obtain phase error adjustment values for the  $m$  clock phases, and wherein  $n$  of the modulo binning devices perform modulo binning of the phase error

16 indications associated with the outputs of the  $n$  sampling devices to obtain phase error  
17 adjustment values for the  $n$  clock phases; and  
18 phase shifting circuitry of the first multi-phase system configured to shift the  
19  $m$  clock phases in accordance with the phase error adjustment values obtained for the  
20  $m$  clock phases.

1 20. The apparatus of claim 19, wherein the first multi-phase system is a receiver  
2 and wherein the second multi-phase system is a transmitter, and wherein  $m$  is an odd  
3 number that is equal to or greater than 3.

1 21. The apparatus of claim 19, wherein the first multi-phase system is a receiver  
2 that includes routing logic configured to cause the phase error adjustment values  
3 obtained for the  $n$  clock phases to be sent to said second multi-phase system, the  
4 second multi-phase system corresponding to a remote transmitter, and wherein the  
5 first data signal sampled by said  $n$  sampling devices corresponds to a signal  
6 transmitted by the remote transmitter.

1 22. The apparatus of claim 19, wherein the first multi-phase system is a  
2 transceiver, the transceiver comprising a local receiver and a local transmitter, the  
3 second multi-phase system corresponding to said local transmitter, the transceiver  
4 including routing logic configured to cause the phase error adjustment values obtained  
5 for the  $n$  clock phases to be sent to said second multi-phase system, and wherein the  
6 first data signal sampled by said  $n$  sampling devices corresponds to a signal  
7 transmitted by the local transmitter.

1 23. An apparatus for controlling sampling operations in a first multi-phase system  
 2 and in a second multi-phase system, the first multi-phase system comprising a first  
 3 multi-phase clock signal generator that generates  $m$  clock signals of  $m$  different  
 4 phases, the second multi-phase system comprising a second multi-phase clock signal  
 5 generator that generates  $n$  clock signals of  $n$  different phases,  $m$  and  $n$  being integers  
 6 that are relatively prime, the apparatus comprising:

7  $n$  sampling devices of the first multi-phase system, each of the sampling  
 8 devices sampling a data signal of the second multi-phase system when one of the  $m$   
 9 clock phase is received by the sampling device and outputting an output signal, and  
 10 wherein  $n$  is equal to or greater than 3;

11 phase error determination circuitry of the first multi-phase system, the phase  
 12 error determination circuitry being configured to determine a phase error indication  
 13 associated with each output of the sampling devices;

14  $m + n$  modulo binning devices, wherein  $m$  of the modulo binning devices  
 15 perform binning of the phase error indications associated with the outputs of the  $m$   
 16 sampling devices to obtain phase error adjustment values for the  $m$  clock phases, and  
 17 wherein  $n$  of the modulo binning devices perform modulo binning of the phase error  
 18 indications associated with the outputs of the  $n$  sampling devices to obtain phase error  
 19 adjustment values for the  $n$  clock phases; and

20 phase shifting circuitry of the first multi-phase system configured to shift the  
 21  $m$  clock phases in accordance with the phase error adjustment values obtained for the  
 22  $m$  clock phases; and

23 phase shifting circuitry of the second multi-phase system configured to shift  
 24 the  $n$  clock phases in accordance with the phase error adjustment values obtained for  
 25 the  $n$  clock phases.

1 24. The apparatus of claim 23, wherein the first multi-phase system is a local  
 2 receiver and the second multi-phase system is a remote transmitter, the apparatus  
 3 being included in the first multi-phase system, and wherein the apparatus further  
 4 comprises routing logic configured to cause the phase error adjustment values  
 5 obtained for the  $n$  clock phases to be sent to said second multi-phase system.

25. The apparatus of claim 23, wherein the first multi-phase system is a transceiver comprising a local receiver and a local transmitter, the second multi-phase system corresponding to the local transmitter, the transceiver including routing logic configured to cause the phase error adjustment values obtained for the  $n$  clock phases to be sent to said local transmitter to be used by the phase shifting logic of the local transmitter to shift the  $n$  clock phases in accordance with the phase error adjustment values obtained for the  $n$  clock phases.

26. The apparatus of claim 23, wherein the phase error determination logic comprises logic that determines phase errors based on an Alexander Phase Determination Truth Table algorithm.

27. The apparatus of claim 23, wherein the modulo binning of the phase error indications is performed by delivering the phase error indications to respective charge pumps of the modulo binning devices in a round robin fashion.

28. A method for controlling clock phases in a multi-phase system, the multi-phase system comprising a multi-phase clock signal generator that generates at least a first clock signal having a first phase, a second clock signal having a second phase, and a third clock signal having a third phase, the first, second and third phases being different from each other, the method comprising the steps of:

sampling a first data signal with a first sampling device when the first clock signal is received by the first sampling device and outputting a first output signal from the first sampling device;

sampling the first data signal with a second sampling device when the first clock signal is received by the second sampling device and outputting a second output signal from the second sampling device;

sampling the first data signal with a third sampling device when the first clock signal is received by the third sampling device and outputting a third output signal from the third sampling device;

determining at least a first phase error indication associated with the first output signal, a second phase error indication associated with the second output signal and a third phase error indication associated with the third output signal;



18           shifting at least one of the first, second or third phases in accordance with the  
19   respective first, second or third phase error indications.

1   29.    The method of claim 28, further comprising the step of:  
2           phase-locking the multi-phase clock signal generator in accordance with the  
3   first phase error indication, and wherein the shifting step includes shifting at least the  
4   second and third phases in accordance with the second and third phase error  
5   indications, respectively.

1   30.    The method of claim 28, further comprising the step of:  
2           phase-locking the multi-phase clock signal generator in accordance with the  
3   first, second and third phase error indications, and the shifting step includes shifting  
4   the first, second and third phases in accordance with the first, second and third phase  
5   error indications, respectively.

1   31.    The method of claim 30, wherein the step of shifting the first and second  
2   phases includes utilizing at least first and second charge pumps to perform modulo  
3   binning of the first and second phase error indications, respectively, to obtain first and  
4   second phase shifting values and shifting the first and second phases in accordance  
5   with the obtained first and second phase shift values, respectively.

1   32.    The method of claim 28, wherein the phase errors are determined based on an  
2   Alexander Phase Determination Truth Table algorithm.

1   33.    A method for sampling signals in a first multi-phase system, the first multi-  
2   phase system comprising a multi-phase clock signal generator that generates  $m$  clock  
3   phases, each clock phase being different, the method comprising the steps of:  
4           sampling a first data signal with  $n$  sampling devices, wherein  $n$  corresponds to  
5   a number of clock phases of a second multi-phase system and wherein  $m$  and  $n$  are  
6   integers that are relatively prime and  $n$  is equal to or greater than 3, each sampling  
7   device sampling the first data signal when one of the  $m$  clock signals is received by  
8   the respective sampling device and outputting an output signal;  
9           determining a phase error indication associated with each output of the  $n$   
10   sampling devices;

11 utilizing  $m + n$  modulo binning devices to perform binning of the phase error  
 12 indications associated with the outputs of the  $m + n$  sampling devices to obtain phase  
 13 error adjustment values for the  $m$  clock phases and phase error adjustment values for  
 14 the  $n$  clock phases; and  
 15 shifting the  $m$  clock phases in accordance with the phase error adjustment  
 16 values obtained for the  $m$  clock phases.

1 34. The method of claim 33, wherein the first multi-phase system is a receiver that  
 2 includes routing logic configured to cause the phase error adjustment values obtained  
 3 for the  $n$  clock phases to be sent to said second multi-phase system, the second multi-  
 4 phase system corresponding to a remote transmitter, and wherein the first data signal  
 5 sampled by said  $n$  sampling devices corresponds to a signal transmitted by the remote  
 6 transmitter.

1 35. The method of claim 33, wherein the first multi-phase system is a transceiver,  
 2 the transceiver comprising a local receiver and a local transmitter, the transceiver  
 3 including routing logic configured to cause the phase error adjustment values obtained  
 4 for the  $n$  clock phases to be sent to said second multi-phase system, the second multi-  
 5 phase system corresponding to said local transmitter, and wherein the first data signal  
 6 sampled by said  $n$  sampling devices corresponds to a signal transmitted by the local  
 7 transmitter.

1 36. A method for controlling sampling operations in a first multi-phase system  
 2 and in a second multi-phase system, the first multi-phase system comprising a first  
 3 multi-phase clock signal generator that generates  $m$  clock phases, each clock phase  
 4 being different, the second multi-phase system comprising a second multi-phase clock  
 5 signal generator that generates  $n$  clock phases, each of the  $n$  clock phases being  
 6 different,  $m$  and  $n$  being integers that are relatively prime, the method comprising the  
 7 steps of:

8 sampling a data signal  $n$  sampling devices, each of the  $n$  sampling devices  
 9 sampling the data signal upon receiving one of the  $m$  clock signals and outputting an  
 10 associated output signal, and wherein  $n$  is equal to or greater than 3;  
 11 for each output signal, determining a corresponding phase error indication;

12           binning the phase error indications modulo  $m$  to obtain phase error adjustment  
 13 values for the  $m$  clock phases;  
 14           binning the phase error indications modulo  $n$  and to obtain phase error  
 15 adjustment values for the  $n$  clock phases; and  
 16           shifting the  $m$  clock phases in accordance with the phase error adjustment  
 17 values obtained for the  $m$  clock phases; and  
 18           shifting the  $n$  clock phases in accordance with the phase error adjustment  
 19 values obtained for the  $n$  clock phases.

1   37.    A method for sampling data in multi-phase sampling system having an odd  
 2 number of clock phases, the clock phases being generated by a multi-phase clock  
 3 generator, the method comprising the steps of:  
 4           using an odd number of samplers to sample a common input signal, each  
 5 sampler sampling the input signal when a clock signal of one of said phases is  
 6 received thereby, each of the sampling devices outputting a respective output signal.

1   38.    The method of claim 37, further comprising the steps of:  
 2           receiving the respective output signals and making a respective phase error  
 3 determination based on each of the respective output signals.

1   39.    The method of claim 38, further comprising:  
 2           shifting one or more of the phases in accordance with the respective phase  
 3 error determinations.

1   40.    A computer program for reducing clock phase errors in a multi-phase system,  
 2 the computer program being embodied on a computer-readable medium, the multi-  
 3 phase system comprising a multi-phase clock signal generator that generates at least a  
 4 first clock signal having a first phase, a second clock signal having a second phase,  
 5 and a third clock signal having a third phase, the first, second and third phases being  
 6 different from each other, wherein first, second and third sampling devices of the  
 7 multi-phase system sample a first data signal upon receiving the first, second and third  
 8 clock signals, respectively and outputting first, second and third output signals,  
 9 respectively, the computer program comprising:

10           a first code segment for processing the first, second and third output signals  
 11   and determining first, second and third phase error indications associated with the  
 12   first, second and third output signals, respectively; and  
 13           a second code segment for determining an amount by which at least one of the  
 14   first, second and third phases are to be shifted based on the first, second or third phase  
 15   error indications, respectively.

1   41.    The computer program of claim 40, wherein the first code segment  
 2   corresponds to an Alexander Phase Determination Truth Table algorithm.

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